Reg. No. :

Question Paper Code : 71738

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2017.

Sixth/Seventh/Eighth Semester

Electronics and Communication Engineering

EC 6601 — VLSI DESIGN

(Common to Biomedical Engineering/B.E. Electrical and Electronics Engineering/ B.E. Electronics and Communication Engineering/B.E. Electronics and Instrumentation Engineering/B.E. Medical Electronics Engineering/ B.E. Robotics and Automation Engineering)

(Regulations 2013)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is meant Channel length modulation in NMOS transistors?

2. Define propagation delay of a CMOS inverter.

3. Define Elmore constant.

4. State the advantages of transmission gates.

5. What is meant by pipelining?

6. Compare and contrast synchronous design and asynchronous design.

7. List out the components of data path.

8. Give the application of high speed adder.

9. What is meant by CBIC?

10. Name the elements in a Configuration Logic Block.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Draw and explain the DC and transfer characteristics of a CMOS inverter with necessary conditions for the different regions of operation. (8)

(ii) Draw the layout diagram for NAND and NOR gate. (8)

Or

(b) Explain the need of scaling, scaling principles and fundamental units of CMOS inverter. (16)

12. (a) (i) Explain about DCVSL logic with suitable example. (10)

(ii) What is transmission gate? Explain the use of transmission gate. (6)

Or

(b) Explain the static and dynamic power dissipation in CMOS circuits with necessary diagrams and expressions. (16)

13. (a) (i) Explain the operation of True Single Phase Clocked Register. (8)

(ii) Draw and explain the operation of Conventional, pulsed and resettable latches. (8)

Or

(b) Explain the concept of timing issues and pipelining. (16)

14. (a) (i) Explain the concept of carry look ahead adder with neat diagram. (10)

(ii) Discuss the details about speed and area trade off. (6)

Or

(b) Explain the concept of modified Booth multiplier with a suitable example. (16)

15. (a) Explain about different types of ASIC with neat diagram. (16)

Or

(b) (i) Explain about building block architecture of FPGA. (10)

(ii) Write short notes on routing procedures involved in FPGA interconnect. (6)

———————